REMARKS/ARGUMENTS

Applicants have received the Office Action dated April 18, 2007, in which the Examiner: 1) rejected claims 1, 4-8, 18 and 21-22 under 35 U.S.C. § 101 because the claimed invention is allegedly directed to non-statutory subject matter; and 2) rejected claims 1, 4-9, 12-13, 15-18 and 21-22 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Mallick et al. (U.S. Pat. No. 5,752,014, hereinafter "Mallick") in view of Intel's *Intel® IA-64 Architecture Software Developer's Manual Volume 1:IA-64 Application Architecture*, (hereinafter referred to as "Intel Volume 1") and further in view of Blaner et al. (U.S. Pat. No. 5,649,178, hereinafter "Blaner"). With this Response, Applicants have amended claims 1 and 18. Based on the amendments and arguments contained herein, Applicants believe this case to be in condition for allowance.

I. REJECTIONS UNDER 35 U.S.C. § 101

The Examiner rejected claim 1 under § 101. The Examiner stated that there is no recitation as to "how the static branch prediction instruction would influence the system during execution, since the claim language is not concrete on the instruction's affects on the system, since all it does is 'provide prediction information.' " Without regard to the merits of the Examiner's comments, Applicants have amended claim 1 to specify that the processor "predicts one or more condition branch instructions by executing said static branch prediction instructions." This added language certainly specifies how the instruction would influence the system during execution. Applicants believe the Examiner's concerns have been addressed by this amendment and thus Applicants request the Examiner to withdraw the § 101 rejection of claims 1 and 4-8.

With regard to claim 18, the Examiner stated that "[t]here is nothing in the claim stating what occurs when the decoded instruction is not a branch prediction software instruction." Applicants have addressed this comment by adding an additional limitation to claim 18 to specify what happens if the decoded instruction is not a branch instruction. Applicants have also amended claim 18 to specify that, if the decoded instruction is a branch prediction software instruction, the method comprises "predicting at least one conditional branch instructing based on

the branch prediction information." This limitation imparts an additional tangible result.

II. REJECTIONS UNDER 35 U.S.C. § 103(a)

Claim 1 is directed to a system comprising a processor that executes a particular kind of static branch prediction instruction; specifically, a static branch prediction instruction that comprises "a plurality of groups of static branch prediction bits, each group being configurable to provide prediction information for a separate conditional branch instruction." The Examiner apparently concedes that Mallick does not teach the quoted limitation. Instead, the Examiner uses Intel Volume I and Blaner.

Intel Volume I teaches a branch prediction instruction that provides prediction information for only one branch conditional instruction. In the Examiner's "Response to Arguments" (Office Action page 11), the Examiner stated, with regard to Intel Volume I, that "[w]hether it is one branch or multiple branches does not matter. As Intel teaches...multiple prediction branches contain the same information and affect the system the same as Applicants' single instruction." Applicants disagree. Intel Volume I simply does not teach the quoted limitation of claim 1. Further, one of ordinary skill would not likely be of the opinion that an instruction, as in claim 1, that encodes multiple groups of static branch prediction bits, each group being configurable to provide prediction information for a separate conditional branch instruction, to be obvious in light of multiple instructions, each instruction providing prediction information for only a single conditional branch instruction. The invention of claim 1 is a different and more efficient way to encode branch prediction information than is taught by Intel Volume I.

With regard to Blaner, Blaner provides an improvement to hardware-based conditional branch instructions predictors. More specifically and with reference to Figure 1, the "[c]ache/BHT[1] 102 provides temporary storage for lines of data received from memory 100 and also provides branch history bits for branch

[1] "BHT" stands for Branch History Table. Col. 3, lines 9-10.

instructions contained within the data. Thus, cache/BHT 102 provides for dynamic prediction of branch outcomes by tagging branch instructions in the cache with predictive information regarding their outcomes... ." Col. 3, ll. 10-18. Blaner does not teach or suggest that "static branch prediction instructions comprise a plurality of groups of static branch prediction bits, each group being configurable to provide prediction information for a separate conditional branch instruction." Blaner does not even teach or suggest the use of processor-executed static branch prediction instructions. Instead, Blaner teaches the use of dynamic branch prediction hardware. Thus, Blaner does not satisfy the deficiency of Mallick or Intel Volume I.

The Examiner also stated that "[s]imply adding a plurality of operand fields to an instruction is not a patentable feature if only because Applicants would be claiming in instruction and the instruction's format, both of which are non-statutory subject matter. Applicants have addressed the Examiner's § 101 rejections (see above) in a manner that also addresses this point made by the Examiner.

The Examiner also alleged that claim 1 provides "intended use" language which the Examiner believes is not limiting subject matter. Without regard to the merits of the Examiner's comments, Applicants' amendments to claim 1 addresses the Examiner's concerns on this point.

For at least these reasons, claim 1 and its dependent claims are allowable over the art of record.

Claim 9 refers to a static branch prediction instruction that provides "separate static branch prediction information about a plurality of conditional branch instructions." The Examiner correctly concedes that Mallick does not teach such static branch prediction instructions. As explained above, Intel Volume 1 does not teach a branch prediction instruction that comprises prediction information about multiple conditional branch instruction, and multiple individual branch prediction instructions that each provide prediction information about only one conditional branch instruction is substantially different from the claimed subject matter. Further, Blaner does not teach or suggest the quoted limitation above. Instead, Blaner teaches the use of dynamic branch prediction hardware,

not a static branch prediction instruction as claimed. Thus, none of the art of record teaches or suggests a static branch prediction instruction that provides "separate static branch prediction information about a plurality of conditional branch instructions." Mallick and Blaner are not directed to branch prediction instructions and Intel Volume 1 discloses the use of a branch prediction instruction that can provide prediction information for only one branch instruction. For at least these reasons, claim 9 and its associated dependent claims are allowable over the art of record.

Claim 18 is directed to a method that requires, among other actions, "including a static branch predictor software instruction in a program, said branch prediction software instruction including branch prediction information configurable to pertain to a plurality of conditional branch instructions in the program." The Examiner correctly conceded that Mallick does not teach such branch prediction instructions. As explained above, none of the art of record teaches or suggests a branch prediction instruction that includes "branch prediction information configurable to pertain to a plurality of conditional branch instructions." Mallick and Blaner are not directed to branch prediction instructions and Intel Volume 1 discloses the use of a branch prediction instruction that can provide prediction information for only one branch instruction. For at least these reasons, claim 18 and its associated dependent claims are allowable.

III. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees

are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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